Amendments to the Claims

Please replace the Claims as shown below:

1. (Currently Amended) A network device comprising:

a first central processing unit (CPU), wherein said first CPU is integrated within said network device;

an input interface comprising a microcontroller for controlling operation of said input interface, said input interface is coupled to said first CPU, said input interface for receiving a plurality of packets ~~coupled to said first CPU~~, said input interface comprising ~~at least one input port~~ a plurality of input ports wherein at least one [[said]] input port of said plurality of input ports is configured to sample at least one input packet and transmit a sampled input packet to said first CPU, said microcontroller of said input interface is coupled to said plurality of input ports, wherein at least one [[said]] input port of said plurality of input ports comprises a countdown register, and wherein said input port is configured to sample a packet according to said countdown register, said countdown register operates by counting incoming packets;

a second CPU that is integrated within said network device;

an output interface comprising a microcontroller for controlling operation of said output interface, said input interface is coupled to said second CPU, said output interface for transmitting a plurality of packets ~~coupled to said second CPU~~, said output interface comprising ~~at least one output port~~ a plurality of output ports wherein at least one [[said]] output port of said plurality of output ports is configured to sample at least one output packet and transmit a sampled output packet to said second CPU, said microcontroller of said output interface is coupled to said plurality of output ports, wherein at least one [[said]] output port of said plurality of output ports comprises a countdown register, and wherein said output port is configured to sample a packet according to said countdown register, said countdown register operates by counting outgoing packets; and

wherein a packet can travel between said input interface and said output interface.

Claims 2 and 3 (Canceled)

4. (Previously Presented) A network device as recited in Claim 1 wherein said first CPU transmits said sampled input packet to a central control station over a network.

5. (Original) A network device as recited in Claim 4 wherein said central control station comprises a statistical monitoring station.

6. (Original) A network device as recited in Claim 1 wherein said sampled input packet comprises an identification of said input port that sampled said sampled input packet.

7. (Original) A network device as recited in Claim 1 wherein said sampled output packet comprises an identification of said output port that sampled said sampled output packet.

8. (Previously Presented) A network device as recited in Claim 4 wherein said network comprises a local area network.

9. (Previously Presented) A network device as recited in Claim 1 wherein said countdown register is a random number countdown register.

10. (Currently Amended) A method of sampling a packet comprising:

receiving a plurality of packets at an input network circuit of a network device, said input network circuit comprising ~~at least one input port~~ a plurality of input ports, said input network circuit comprising a microcontroller for controlling operation of said input network circuit, said microcontroller of said input network circuit is coupled to said plurality of input ports;

sampling at least one input packet at ~~said input port~~ an input port of said plurality of input ports, wherein said sampling comprises using a countdown circuit;

transmitting at least one sampled input packet to a processor of said network device, wherein said processor is integrated within said network device;

transmitting at least one packet from said input network circuit to an output network circuit of said network device over a switching fabric of said network device,

said output network circuit comprising a plurality of output ports, said output network circuit comprising a microcontroller for controlling operation of said output network circuit, said microcontroller of said output network circuit is coupled to said plurality of output ports, wherein said input network circuit and said output network circuit feed into said processor;

sampling multiple output packets simultaneously at said plurality of output ports, wherein said sampling comprises using a plurality of countdown circuits, wherein each of said plurality of output ports comprises one of said plurality of countdown circuits; and

transmitting said multiple sampled output packets to said processor and a second processor.

11. (Canceled)

12. (Previously Presented) A method as recited in Claim 10 wherein said countdown circuit is a random number countdown circuit.

Claims 13 and 14 (Canceled)

15. (Original) A method as recited in Claim 10 further comprising said processor transmitting said sampled input packet to a statistical monitoring station over a network.

16. (Previously Presented) A method as recited in Claim 10 wherein said network device is an application specific integrated circuit (ASIC).

17. (Previously Presented) A method as recited in Claim 10 wherein said sampled input packet comprises information regarding said input port performing said sampling at least one input packet at said input port.

18. (Previously Presented) A method as recited in Claim 10 wherein each of said sampled multiple output packets comprises a bitmask regarding which of said plurality of output ports performed said sampling.

19. (Currently Amended) A network device for sampling a packet comprising:

processing means, wherein said processing means is integrated into said network device;

input interface means for receiving a plurality of packets over a network, said input interface means ~~for receiving a plurality of packets~~ comprising ~~an input means~~ a plurality of input means for sampling at least one packet [[and]], said input interface means comprising a microcontroller for controlling operation of said input interface means, said microcontroller of said input interface means is coupled to said plurality of input means, said input interface means for transmitting a sampled incoming packet to said processing means, said input interface means ~~for receiving a plurality of packets~~ coupled to said processing means;

output interface means for transmitting a plurality of packets over said network, said output interface means ~~for transmitting a plurality of packets~~ comprising a plurality of output means for sampling multiple output packets simultaneously [[and]], said output interface means comprising a microcontroller for controlling operation of said output interface means, said microcontroller of said output interface means is coupled to said plurality of output means, said input interface means for transmitting said multiple sampled output packets to said processing means and a second processing means, wherein each of said plurality of output means comprises a countdown means, wherein at least one ~~said input means~~ input means of said plurality of input means comprises a countdown means, and wherein said input means is configured to sample a packet of said plurality of packets according to said countdown means; and

switching means coupled to said input interface means ~~for receiving a plurality of packets~~ and said output interface means ~~for transmitting a plurality of packets~~, said switching means for transmitting a packet between said input interface means ~~for receiving a plurality of packets~~ and said output interface means ~~for transmitting a plurality of packets~~.

Claims 20 and 21 (Canceled)

22. (Previously Presented) A network device as recited in Claim 19 wherein said processing means transmits said sampled incoming packet to a central control means over a network.

23. (Currently Amended) A network device comprising:

a first processor integrated within said network device;

a second processor integrated within said network device;

a switching fabric;

an input interface coupled to said switching fabric, said input interface comprising a plurality of input ports, said input interface is coupled to said first processor, said input interface comprising a microcontroller for controlling operation of said input interface, said microcontroller of said input interface is coupled to said plurality of input ports, said input interface for sampling at least one incoming packet received at one of said plurality of input ports, wherein each of said plurality of input ports comprises a countdown register, said input interface for transmitting said sampled incoming packet to said first processor;

an output interface coupled to said switching fabric, said output interface comprising a plurality of output ports, said output interface is coupled to said first processor and said second processor, said output interface comprising a microcontroller for controlling operation of said output interface, said microcontroller of said output interface is coupled to said plurality of output ports, said output interface for sampling multiple outgoing packets simultaneously at said plurality of output ports, wherein said sampling comprises using a plurality of countdown circuits, wherein each of said plurality of output ports comprises one of said plurality of countdown circuits, said output interface for transmitting said multiple sampled outgoing packets to said processor and a second processor;

a computer-readable memory coupled to said input interface and said output interface; and

wherein a packet can travel between said input interface and said output interface via said switching fabric.

~~a processor coupled to said input interface and said output interface, wherein said processor is integrated into said network device, wherein said input interface and~~

~~said output interface feed into said processor, said processor for executing a method of sampling a packet, said method comprising:~~

~~sampling at least one incoming packet received at one of said plurality of input ports, wherein each of said plurality of input ports comprises a countdown register;~~

~~transmitting said sampled incoming packet to said processor;~~

~~transmitting at least one packet from said input interface to said output interface over said switching fabric;~~

~~sampling multiple outgoing packets simultaneously at said plurality of output ports, wherein said sampling comprises using a plurality of countdown circuits, wherein each of said plurality of output ports comprises one of said plurality of countdown circuits; and~~

~~transmitting said multiple sampled outgoing packets to said processor and a second processor.~~

24. (Currently Amended) A network device as recited in Claim 23 wherein ~~said method further comprises~~ said first processor is for transmitting said sampled incoming packet to a statistical monitoring station over a network.

25. (Previously Presented) A network device as recited in Claim 23 wherein said network device is an application specific integrated circuit (ASIC).